Fermilab - DES
12 Channel CCD Acquisition Board Test Procedures

Revision: 0.1

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Revision History

May 15th, 2008 changes to document
June 19th, 2008 updates to correspond with EXCEL Spreadsheet
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1.0 Introduction

This document covers the testing strategy for the FERMILAB-DES 12 CHANNEL CCD Acquisition Board to take the board from post-assembly to a fully functional state. All tests described in this document pertain to the latest hardware revision level of the subject board. The test procedure assumes that the tester is familiar with the use of the MEC (MONSOON Engineering Console) and can execute the required commands. The tests are divided into progressive stages ranging from 1 to N. Each higher number stage uses assumptions on the board condition that requires the previous stages to have been successfully completed.

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Stage 4. Board fit and Firmware Programming
Stage 5. Power Consumption
Stage 6. Monsoon software system setup
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Stage 12. Front-end Electronics Performance Analysis
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In the description for these tests, certain conventions are followed to ease comprehension. These conventions and examples of each are presented in Table 1.

Table 1 - Test Description Conventions

Convention	Example	Description
Linux commands that are typed on a PAN xterm window	**mecStart**	**Boldface characters**
Commands typed to the MEC command line	***ppxSetAVP***	***Boldface italics***
Buttons on the test chassis boards or MEC console	***>startExp<***	***Bold italics underlined inside > < symbols***
Designate data values that are returned in the PAN xterm or MEC console window	*dir*	*Italics*
Responses from the programs	`this is a response`	`Courier font`
Specific board signal names	**FBIAS1**	**BOLDFACE SMALL CAPITALS**

MEC attribute names	***mcbCodeID***	***Boldface italics***

The tester will record the result of each test in the EXCEL file. When the test results are saved, a file will be created called MNSN-EL-08-0500-SNnnn-xx.btr (where MNSN-EL-08-0500 refers to the board production code, SNnnn is the serial number and xx is the test sequence number for this board. The file extension (.btr) stands for "Board Test Result"). This file should be saved on the local computer in a convenient directory, for example, DES 12 Channel Acquisition/BoardTests. At completion of testing, this file and the generated test report should be copied to the relevant area of the DES document archive: (/MNSN/MonsoonAdmin/Production/TST_Repository/TSTResults/…).

This file is a record of the test and an analysis of the test results that can be printed out and kept in the system binder supplied to the end user. The test procedure functions will request the entry of data as required, data should be filled into the light blue areas of the Excel file.

1.1 Required Equipment

- Test chassis with 6-slot backplane, side panel cutout
- Agilent E3648A dual output DC power supplies(4)
- 12 Channel Transition board
- Monsoon MCB
- Clock Board
- Clock Transition board
- Fermilab Fanout test board V2
- Personal Computer running MS Windows 2000 or Windows XP. The PC must be connected to the network with the \\decapod\MNSN disk mapped into the Windows disk structure. Required programs are MS EXCEL and Xilinx Impact.
- JTAG-programming cable – preferably Xilinx Programming tool Model # DLC9LP
- Oscilloscope - Agilent 7000 series MSO Oscilloscope(MSO 7034A),
- Agilent 33220A 20Mhz Function/Arbitrary Waveform Generator
- Fluke Digital Multimeter.

1.2 Test Schedule

Stage 1. Preparation of Documentation

Step i. If the board under test does not have a serial number, it is up to the user to place one on the board. Local directives will apply. See Figure 1 for serial number location.

Step ii. Create a Microsoft EXCEL file for the board. This document becomes the history of all work carried out on the board after assembly. After the configuration and testing of the board, a printed copy should be made and attached to the circuit board protective box. ***Link to EXCEL TEMPLATE***.

Step iii. Enter the test technician's name into the appropriate entry box and along with the testing date, verify the physical serial number of the board under test. **Print the first six pages of the file.**

Stage 2. Visual Inspection

Step i. Using a comparison photograph or a known good board, visually inspect the board for physical damage, missing and misplaced components. Figures 1and 2 show a typical 12 Channel CCD Acquisition Board.

Step ii. Jumper configuration (JP 1 – JP2), there are two jumpers on the board that should not be installed.

Step iii. Using a Dial Calipers verify that the Board Dimensions are within tolerance using Table 2 for reference.

Table 2.

Board width:	6.299 +/- .05
Board height:	9.187 +/- .05
Board thickness:	0.070 +/- .005

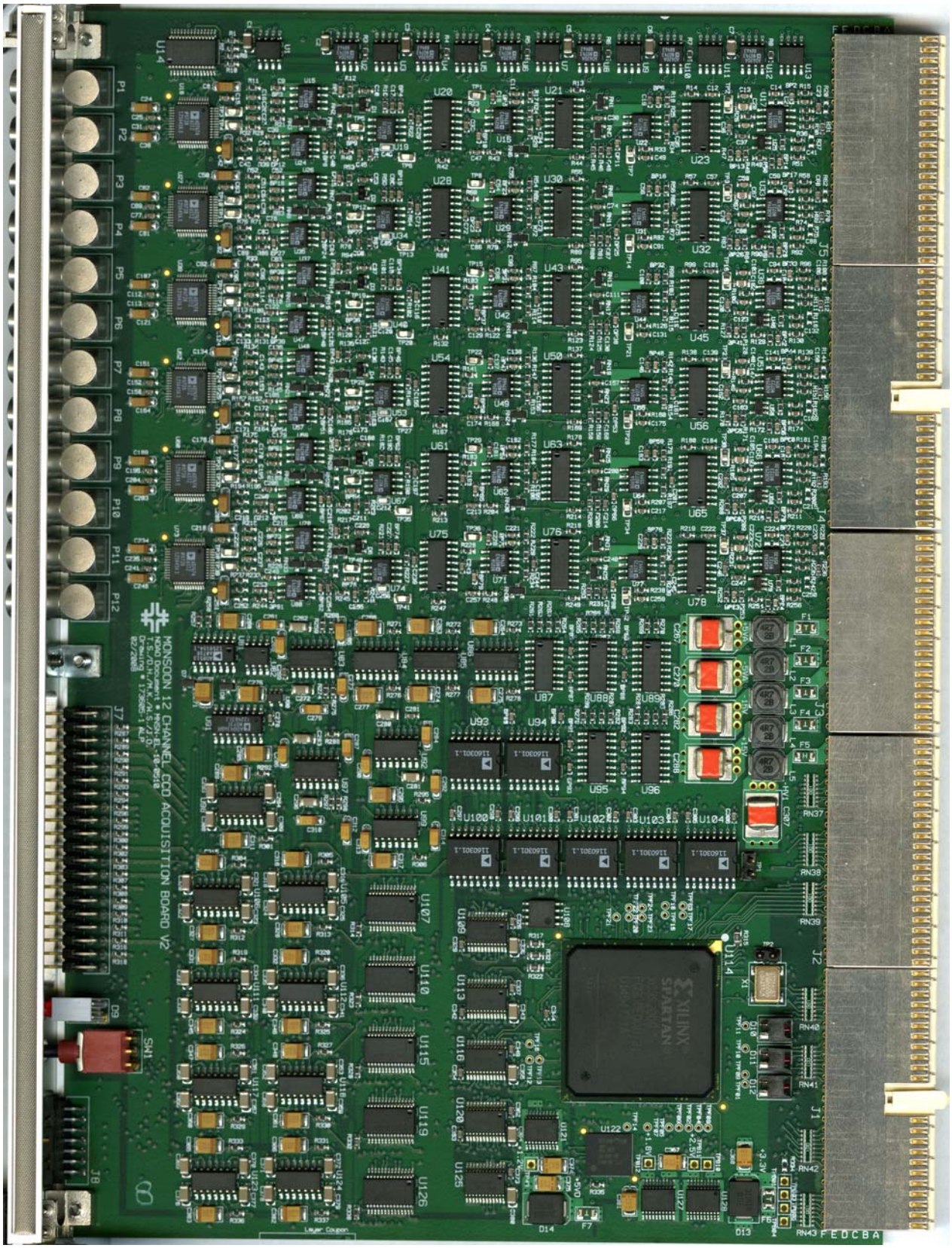

Figure 1: DES 12 Ch Acquisition Board – top view

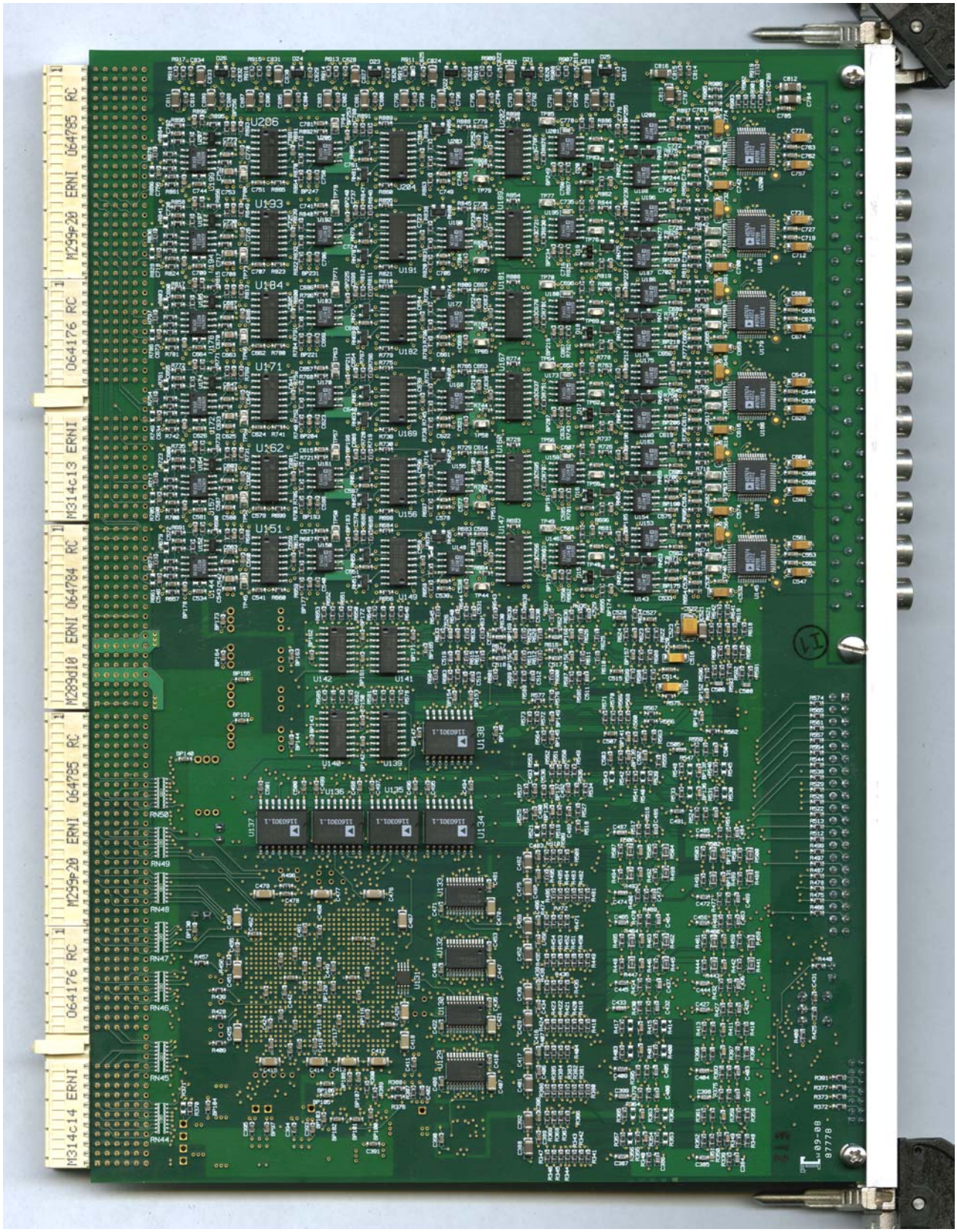

Figure 2: DES 12 Ch Acquisition Board – bottom view

Stage 3. Power Plane "Short" testing

Step i. Using an ohm meter measure the impedance between the power plane and ground plane. Record the value into the EXCEL spreadsheet. The reading should always be above 50 ohm. Refer to Table 3 and Figure 3 for locations to measure the impedance.

Table 3 – Power Plane Impedance measurement nodes

+1.2v digital > measure at TP43 to Bottom side of D13
+1.8v digital > measure at TP12 to Bottom side of D13
+2.5v digital > measure at TP11 to Bottom side of D13
+3.3v digital > measure across D13
+5.0v digital > measure across D14
+5.0v Analog > measure across C267
-5.0v Analog > measure across C270
+15.0v Analog > measure across C288
-15.0v Analog > measure across C282
-28.0v Analog > measure across C307

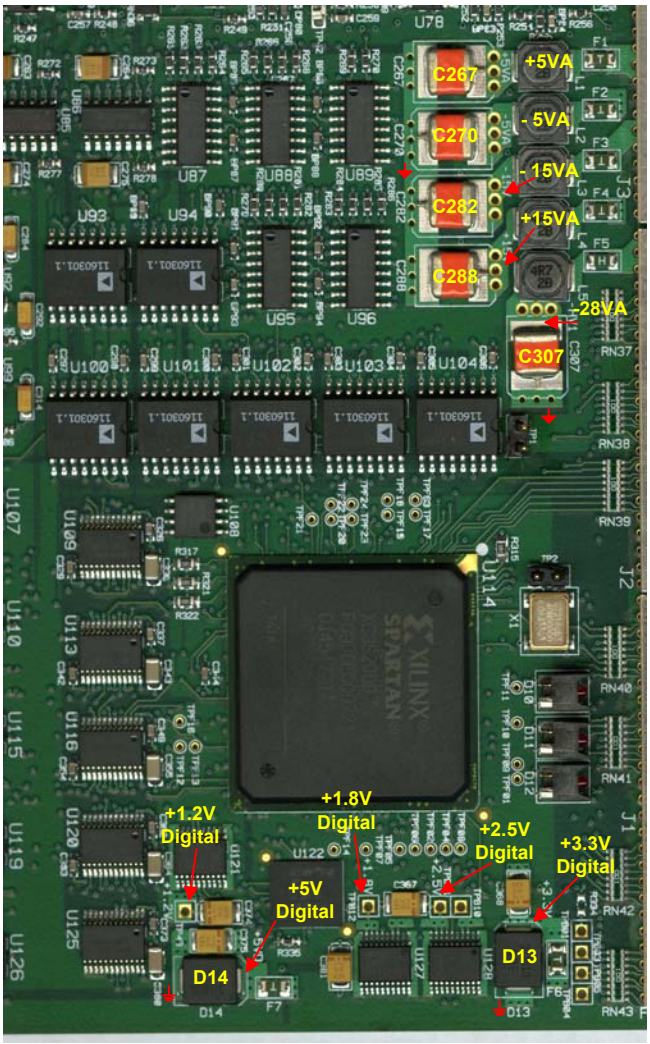

Figure 3: Power Plane measurement nodes - Top View of Board

Stage 4. Board fit and Firmware Programming

Step i. With the power to the test chassis off, carefully insert the new board for the first time in slot 6. While inserting the board, check for the alignment of the connectors and front panel keying if fitted. The 12 channel transition board will need to be in the crate as a means to provide power to the backplane. This should be the only other board in the crate with the board under test at this time.

Step ii. Set the power supply voltages and over-current limits to those listed in Table 6 in Appendix II

Step iii. Apply power to the test chassis by switching on only the +3.3V and +5VD digital supplies.

Step iv. Connect a JTAG programming cable to the JTAG port and the programming pod.

Step v. Initialize the IMPACT JTAG tool. Now follow the procedures outlined in Appendix I to load the field programmable devices. Annotate the firmware filenames and checksum information in the appropriate entry boxes in the EXCEL spreadsheet.

Step vi. Power down the test chassis, wait a second, and re-apply power to the test chassis in the following order: the +3.3V and +5VD digital supplies first, then the +/5VA supplies, then the +/15VA supplies, and finally any +/-HV supplies. This order should be followed whenever applying power to the test chassis. To power down the test chassis, the reverse order should be followed. This assures that the analog circuitry is always under control whenever power is applied or removed.

Step vii. The front panel LED device on the CCD Acquisition board should be illuminated. Press the front panel ***>RESET< button*** on the CCD Acquisition board. The front panel LED should illuminate and then extinguish when the reset switch is released. This shows the FPGA boot circuitry is functioning. During a front panel reset operation, the firmware is reloaded to the FPGA from the EEPROM device.

Stage 5. Power Consumption

Step i. Measure and record the board voltages in the EXCEL spreadsheet. Refer to Table 4 and Figure 4 for locations. The test chassis should have the side panel cut out to allow for measurements on the bottom side of the board. The power supply voltages can be adjusted so that the voltages on the board are at the optimum value. This will allow for compensation of the voltage drop on the power supply cables.

Table 4 – Board Voltage measurement nodes

+1.2v digital > measure at TP43 to Bottom side of D13(Digital Ground)
+1.8v digital > measure at TP12 to Bottom side of D13(Digital Ground)
+2.5v digital > measure at TP11 to Bottom side of D13(Digital Ground)
+3.3v digital > measure at D13 to Bottom side of D13(Digital Ground)
+5.0v digital > measure at D14 to Bottom side of D13(Digital Ground)
+5.0v Analog > measure at C267 to Analog Ground
-5.0v Analog > measure at C270 to Analog Ground
+15.0v Analog > measure at C288 to Analog Ground
-15.0v Analog > measure at C282 to Analog Ground
-28.0v Analog > measure at C307 to Analog Ground

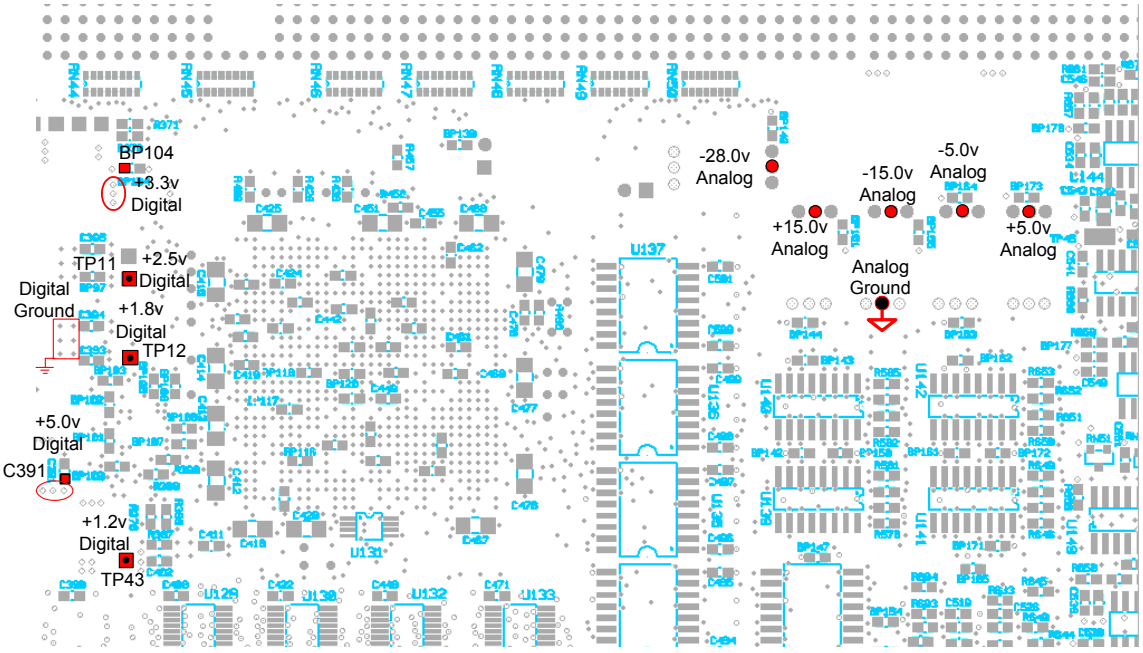

Figure 4: Power Plane measurement nodes - bottom View of Board

Step ii. Record the current consumption from the bench supplies into the EXCEL Spreadsheet.
The current totals will include the 12 Channel board Transition modules current.

Step iii. The power consumption is computed in the EXCEL Spreadsheet, it should be within the following range xxx which is +/- 10 %. The current totals will include the 12 Channel board Transition modules current.

Step iv. Measure and record the Board Reference voltages in the appropriate entry boxes in the EXCEL spreadsheet from measurements taken from the locations shown in figure 5. The reference voltages should be within +/- 1% of the typical value, measure with respect to Analog Ground.

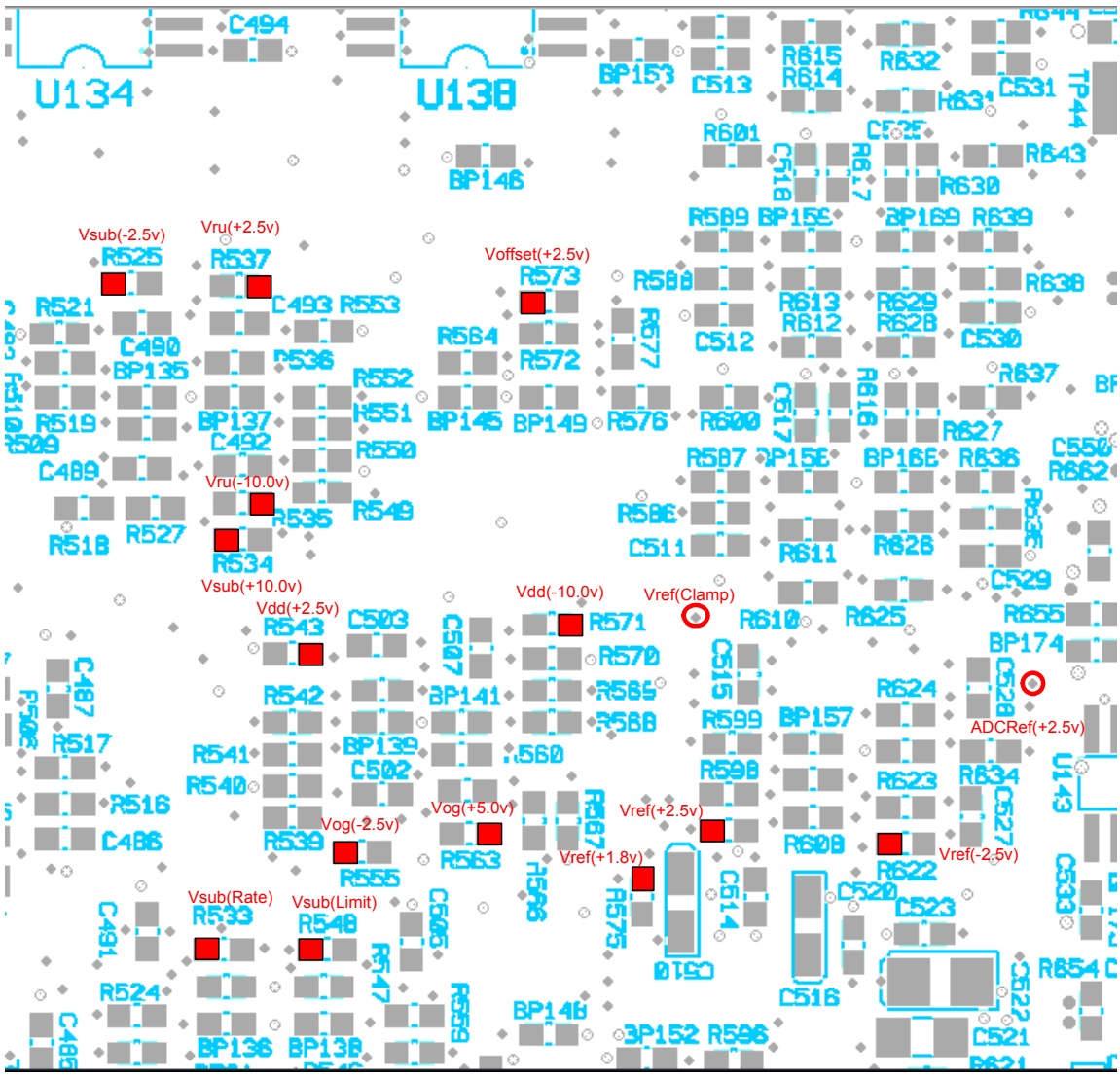

Figure 5: Reference Voltages measurement nodes - bottom View of Board

Step v. Turn the power off to the test chassis in the appropriate order

Stage 6. Monsoon software system setup

Step i. With the power to the crate off insert a Master Control Board(Slot 1) and a Clock board(Slot 3) along with a Clock Transition board into the test chassis. Connect the test cables from the fanout test board to the 12 Channel Transition board located in slot 6 in the rear of the crate. **NOTE:** Slot 1 is marked with a triangle on the PCI back plane and normally has the board guide rails in a unique color.

Step ii. Connect the fibers from the PAN computer to the Master Control Board in slot 1 and power up the supplies to the test chassis in the appropriate order.

Step iii.. Open two xterm windows on the PAN. In the first xterm window, type fs0 and look at the fiber link status. The status will probably show data in the receive FIFO buffer and should show the test chassis to be in reset mode by having the *dir*(ection) bit true in the IO register (*i=01xx0*). The status command should return something similar to the following:

```
FibreXtreme (SL) Monitor (sl_mon) rev. 3.02 (2003/10/06)
Driver: rev. b2-835455:776764 for Linux with API rev. 2.1
Hardware: unit/bus/slot 0/1/4 - SL100 (D64) Firm. 1C.13 (1C.13) for
5.0V PCI
Link Control Register (CSR 0x08) = 0x37
Link Status Register (CSR 0x0c) = 0x200 Link is UP
FPDP Flags Register (CSR 0x10) = 0x200 NR.D.P2.P1.S: i=01110 o=00000
FIFO Threshold Register (CSR 0x14) = 0x0 Int.thr. = 0x0
Data count = 0xE75D (59229) bytes
Link (and other) Errors = 3
Configurable parameters:
Loop Configuration: 0 (Point-to-Point)
Max Timeout: 600000 (6000000 ms)
Flow Control: 0 (NO) Halt on link error: 1 (YES)
CRC generate/check: 1 (YES) Allow Queuing on link error:
```

Figure 6: Link status screen shot

Step iv. Use the command fc0 to clear the read buffer. Confirm with the status command that the read FIFO buffer is now empty (*Data count = 0x0 (0) bytes*) and that no link errors persist.

NOTE: Before proceeding with Step v, know what the PAN network name is and either create or identify an existing data directory in which to store the acquired data for test analysis. The PAN network name and the data directory name are then substituted in the command for the panMachineName and data variables.

Step v. In the second xterm window, start the PAN software and MONSOON Engineering Console using the command by double clicking the “Start Monsoon” Icon that is on the desktop. A window will appear that allows you to select a focal plane for initializing the system. Select FNAL_12Ch and click the “Start” button.

Step vi. Verify that the text fields “Step 1. Enter Host Name” and “Step 2. Port Number” contain the correct PAN machine name and port number (5142). Press the ***>Connect<*** button on the MEC. The Attribute Display pages will appear. Next press the ***>RESET<*** then the ***>ASYNCRESP<*** buttons on the MEC console. This achieves synchronization of the communication link. You should receive an OK: ppxAsyncResp: Success message in the MEC console message area and the “PIX” and “SEQ” LED’s on the MCB should have been extinguished. Leave the PAN software running.

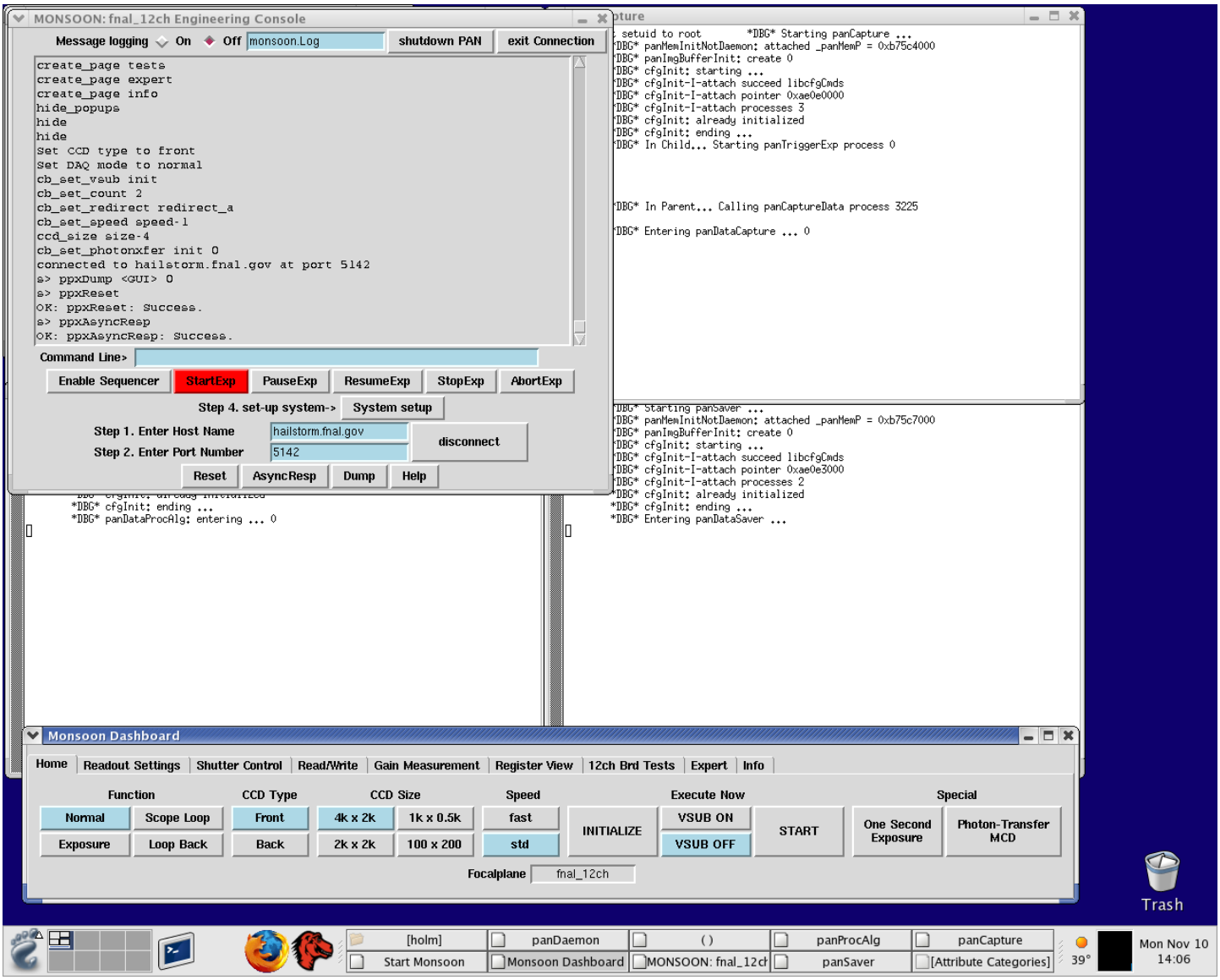

Figure 7: Initial MEC Screen after Connection, >reset> and >asyncResp>

Stage 7. Basic Bus Transactions - Digital Register Tests

Step i. On the MEC , press the **>*RESET*<** then the **>*ASYNCRESP*<** buttons. The front panel LED devices on the MCB should extinguish.

Step ii. On the MONSOON DASHBOARD, select the >**100 x 200 CCD**< size and then press the >**Initialize**< button, this will cause some communication with the 12 Channel Board and the LEDs on the front panels should flash. There is a tab for **>12 Channel board tests<** select this tab and then press the ***>REGISTER TEST<*** button, a new window will appear. Select the ***>TEST ALL REGS<*** button to select all the registers, followed by the ***>Pattern TEST<*** this test will take a few minutes. Press the type of test buttons in order "Pattern", "Walking 1's", "Walking 0's". If the test passes circle "Passed" in the EXCEL Spreadsheet. If the test fails test each Register separately and record pass or fail along with placing an X in the bit that fails for the particular register. This proves the basic functioning of the 12 Channel Board's clock and sequencer bus operation.

Step iv. Close the REGISTER TEST window and click on the "Home" tab.

Step v. Press the >**Initialize**< button in the MONSOON DASHBOARD to set all registers back to the initialized state.

Stage 8. Bias Voltage Tests

Step i. Power on the oscilloscope and set to 5v vertical deflection, 50ms / x division, and auto trigger.

Step ii. On the MONSOON DASHBOARD, press the ***>12Ch Board TEST<*** tab. Within that window enter the filename that will store the telemetry readback values and select the box. The filename should have some meaning to it, i.e. "Board5_Noverber8_2008". Click on the button marked ***>Bias Voltage Test<***. A window should pop up allowing the bias voltages to be set to 10, 50 or 90% and enabled/disabled.

Step iii. Click on the **>Set Bias Voltages to 10% button<.** Measure each individual Bias voltage on the 12 channel board useing Figure 7 to find the locations on the bottom of the board. Measure to two decimal place precision using a DVM. Measure with respect to Analog Ground. Enter these values into the entry boxes in the EXCEL spreadsheet. The telemetry values of all the Bias voltages for this operation will be written to the log file. After the tests are completed cut and paste the telemetry values from the log file to the EXCEL Spreadsheet.

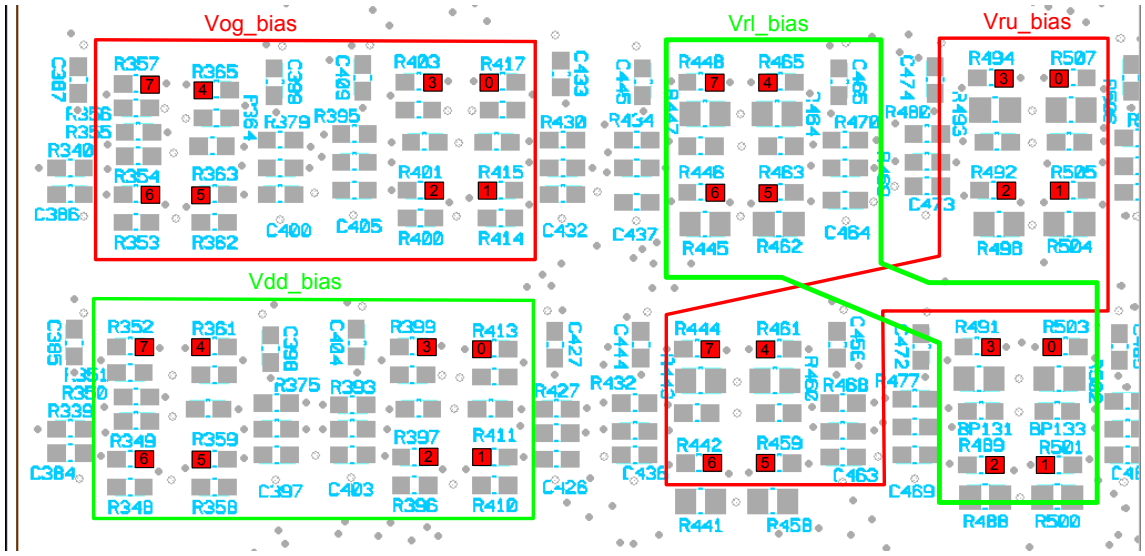

Figure 8: Bias Voltages measurement nodes - bottom View of Board

Step iv. Click on the button marked ***>Set Bias Dacs 50%<***. All Bias voltages will be set to their 50% level. Measure each individual voltage to two decimal place precision on a DVM and enter these values into the entry boxes provided on the EXCEL spreadsheet. The telemetry values of all the Bias voltages for this operation will be written to the log file.

Step v. With all Bias voltages set to their 50% level. Look at each Bias voltage with the oscilloscope to detect any obvious oscillations or ringing behavior. Make a note in the EXCEL Spreadsheet if there are any oscillations in the box provided at the bottom of the table 6. The scope channel should be on the AC setting, 50mv/div, 1us/div.

Step vi. Click on the button marked ***>Set Bias Dacs 90%<***. All Bias voltages will be set to their 90% level. Measure each individual voltage to two decimal place precision on a DVM and enter these values into the entry boxes provided on the EXCEL spreadsheet. The telemetry values of all the Bias voltages for this operation will be written to the log file.

Note: The ***slope and Intercept values*** for each of the bias voltages is computed within the EXCEL Spreadsheet from the means calculated from the previous step. These values are used as calibration constants for the board description file.

Close the current window and return to the 12 Channel board test window, uncheck the box to store data to the LOG file! Return to the Bias Voltage Test window.

Step viii. To measure the rise time for each channel repeatably press the button marked ***>Set Bias Dacs 10%<*** followed by the button marked ***>Set Bias Dacs 90%<.*** Connect the scope to each individual HV bias test point and record the rise time of each channel.

The rise time will change for the 4 different BIAS types and will be in the millisecond range. Vru and Vrl : 5v/Div, 1ms/Div, Vog: 1v/Div, 1ms/Div, Vdd: 5v/Div, 10ms/Div.

Step ix . Click the **>*Set Bias Dacs 90%*<** button. While repeatably pressing the **>*Enable Bias Button*<** monitor the bias voltages on the fanout test board one at a time using the oscilloscope. Each Bias should show a sharp return to AGND as they are disabled and an equally sharp return to their level when enabled. This tests the ability to isolate the biases from a detector. After all biases have been tested, leave the button in the enabled condition for the next test. WE NEED A LOAD ON THE FANOUT BOARD FOR THIS _ WAIT UNTIL THE NEW TRANSISTION BOARDS ARE AVAILABLE. *SCOPE SETUP FILE Put a load on the fanout board!*

THE FOLLOWING TEST SHOULD BE DONE AFTER THE ADC CIRCUITRY IS VALIDATED(Stage 11.)

Step x. On the fanout test board connect up the 6 Vru outputs to 6 of the 12 ADC inputs using the small jumpers. Unclick the write to log file button. Run the Noise test 4 routine,(Click on the button marked **>*Measure Noise*<**. If the noise levels are 4 counts above the typical value then record the Noise levels (STD. Dev. value)displayed on the screen into the Excel file table 6. Measure the Noise for the 6 Vrl rails, 6 Vog rails and 6 Vdd rails in the same manner. The reading should all be less than 4 units above the normal readings of the other 6 ADC channels that are shorted on the fanout board.

Stage 9. Vsub circuitry and Heater control

Step i. In the “12 Channel Board test” window select the “Vsub – Temp button”, a new window will appear. Click the box to save the data to the log file. Click on the 10% button. Measure and record voltages onto the Excel Spreadsheet at the Vsub-Rate, Vsub-Limit and the Vsub0 nodes shown in figure 9. Click the 50% button and record the 3 voltages. Click the 90% button and record the 3 voltages. Test the Vsub enable bit by clicking the “toggle Vsub enable” button. The voltage at Vsub0 should go from the 90% level to ground when the Vsub is disabled. The window will report wether the bit is a “1”(enabled) or “0”(disabled). In the Excel spreadsheet circle pass or fail for the enable bit.
The RTD temperature readings will reflect the value of the resistor that is installed onto the fanout board. The values should match the table shown below.

Table 5. Vsub, RTD & Reference telemetry read back values

	10%	**50%**	**90%**
Vsub1 =>			
Vsub2 =>	-29dec	698dec	1425dec
RTD1 =>	220dec		
RTD2 =>	248dec		
RTD3 =>	274dec		
RTD4 =>	302dec		
RTD5 =>	324dec		
RTD6 =>	349dec		
Reference 4096 =>	837dec		
Buffer Reference =>	837dec		

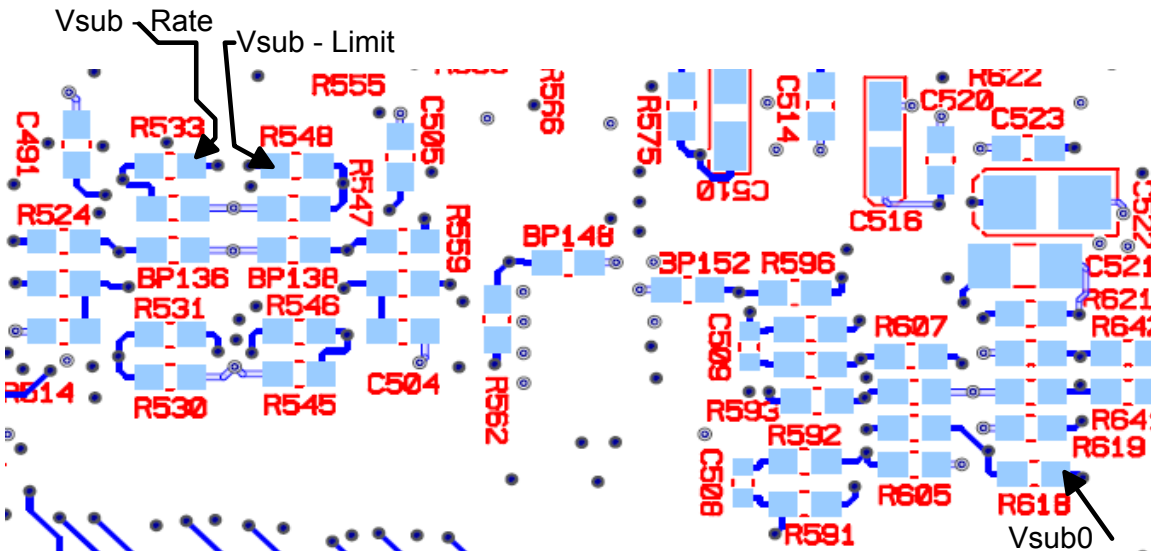

Figure 9: Vsub measurement nodes(3) - bottom View of Board

Stage 10. Video Offset DAC Tests

Step i. In the "12 Channel Board test" window select the ADC Offset button, a new window will appear that allows you to set the ADC offset voltage to 10, 50 or 90%. Using the DMM measure and record the voltage appearing at the Voffset nodes using figure 9 as a reference. The video channel ADC devices are triggered and readings displayed in the window while the video offset DACs are set to 10%, 50% and 90% of their dynamic range, these values are written to the log file to be transferred to the EXCEL spreadsheet later. The ADC readings are used to calculate the slope and intercept of the DAC range in units of ADU. The mean data values returned in the entry boxes should be within 200 ADU of each other and the slope value reasonably consistent.

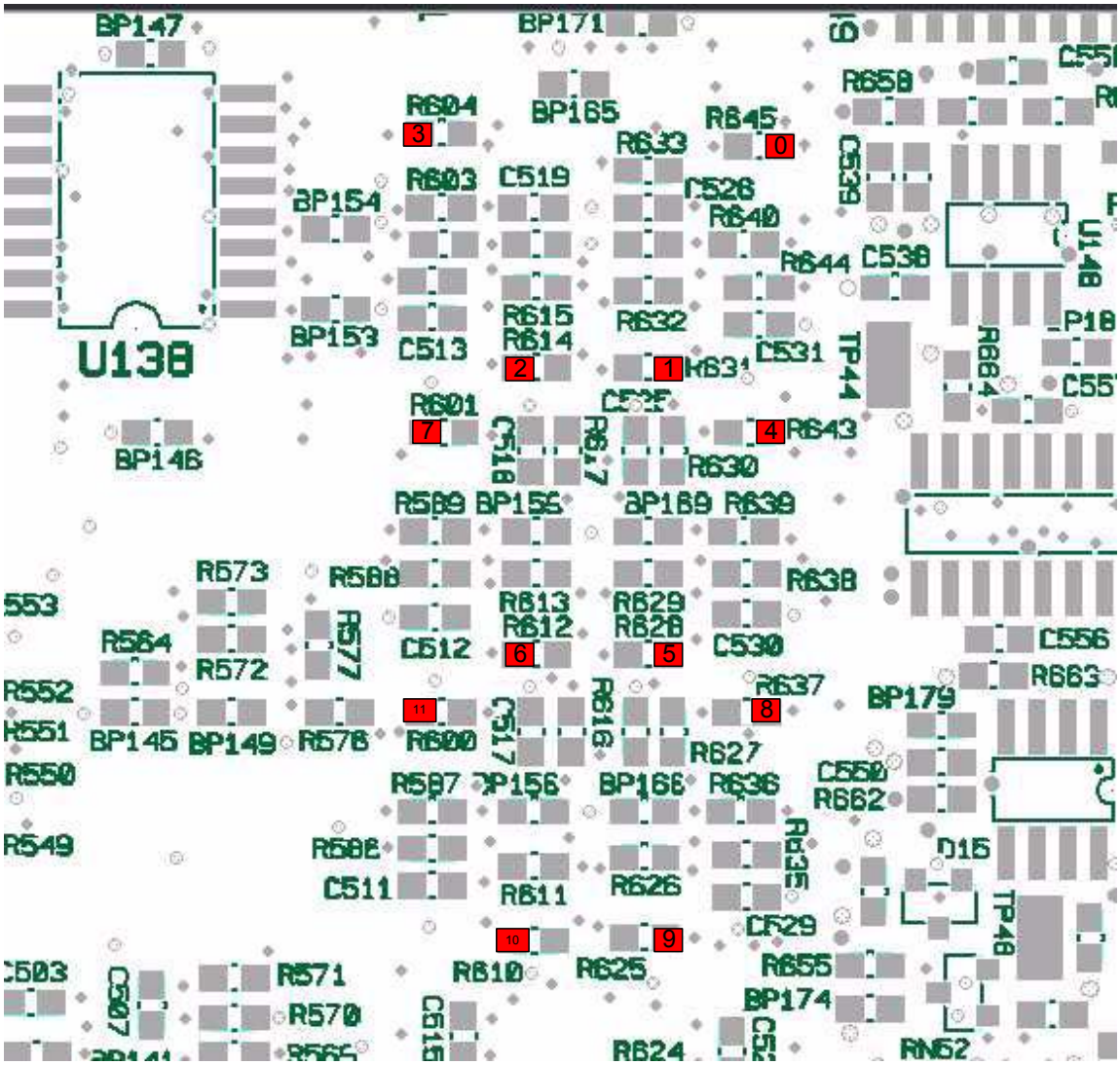

Figure 10: ADC Offset Voltages measurement nodes - bottom View of Board

Step ii. Close the ADC offset window and uncheck the "write to logfile" box. Return to the ADC offset window. Using the oscilloscope check for oscillations on each offset channel when they are set to the 50% level. The scope channel should be on AC setting, 50mv/div, 1us/div. Make a note in the Excel spreadsheet table 8 if there are any oscillations.

Step iii. Measure the risetime of each offset voltage using the oscilloscope. Record the rise time in a manner similar to the Bias voltages by first setting the Offsets to 10% and then recording the rise time when the Offsets are set to 90%. The scope channel should be on DC setting, 500mv/div, 1us/div.

Stage 11. CDS Control Functions and Video Channel Performance Testing.

Step i. Connect the oscilloscope Digital PODS(1-16) to the CCD Acquisition board front panel using Figure 11 and Table 3 as a guide. Recall the setup file "SCOPE_3" from the USB thumb drive. The Fanout test board should have its ADC inputs jumpered to the ADC shield inputs for all 12 channels. In the MEC window select the 100x200 button followed by the Intialize button. Select the ***>12Ch Board TEST<*** tab followed by ***>ADC TEST<*** buttons.

Table 6 - Agilent Oscilloscope MSO Connections

Agilent Oscilloscope Logic Analyzer Pods => 12 Ch Front Panel - J19	
Pod 1	**Pod 2**
D0 => J19 pin 3 > cds_gain	D8 => J19 pin 19 > adc_busy
D1 => J19 pin 5 > cds_dcrestore*	D9 => J19 pin 21 > adc_sync
D2 => J19 pin 7 > cds_integrate*	D10 => J19 pin 23 > adc_sdat
D3 => J19 pin 9 > cds_invert	D11 => J19 pin 25 > PIXEL_XMIT
D4 => J19 pin 11 > cds_noninvert	D12 => J19 pin 4 > Sel_n
D5 => J19 pin 13 > cds_reset*	D13 => J19 pin 6 > seq_mode0
D6 => J19 pin 15 > cds_cnvst*	D14 => J19 pin 10 > seq_addr0
D7 => J19 pin 17 > adc_sclk	D15 => J19 pin 16 > seq_data0
Gnd => J19 pin 1	Gnd => J19 pin 2

CCDACQ12 Front Panel Test Points

(firmware version 201D or newer)

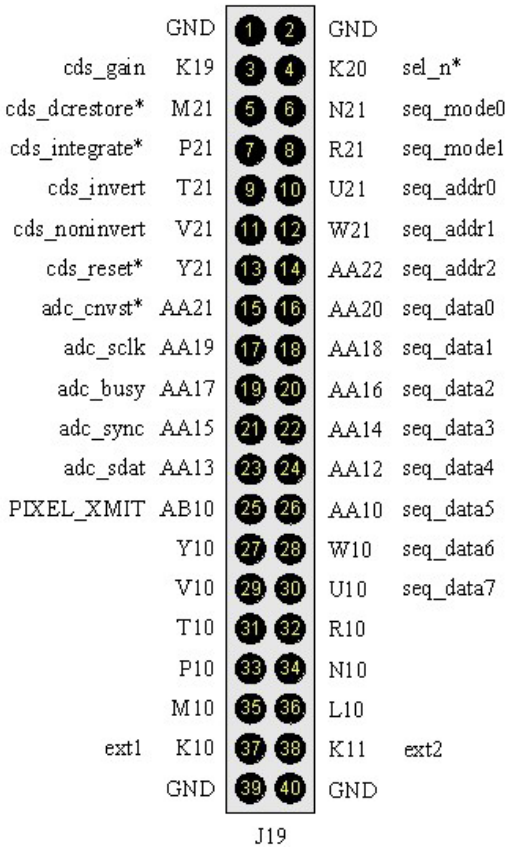

Figure 11 – 12-Ch DES CCD Acquisition Board Front Panel Test Points

Step ii. In the new window that appeared check the box to write the data to the logfile. Press the button marked ***>Noise Test 1<***. This will initiate an acquisition cycle, with the results written to the screen and to the log file. The data from the logfile will eventually be transferred to the EXCEL Spreadsheet. This setup will acquire data from the ADC channels while the CDS circuit is held static. This test verifies the correct operation of the ADC devices and measures the noise of the circuit up to the DC Clamp switch in a static state. The oscilloscope will trigger and display a waveform similar to that shown in Figure 12.

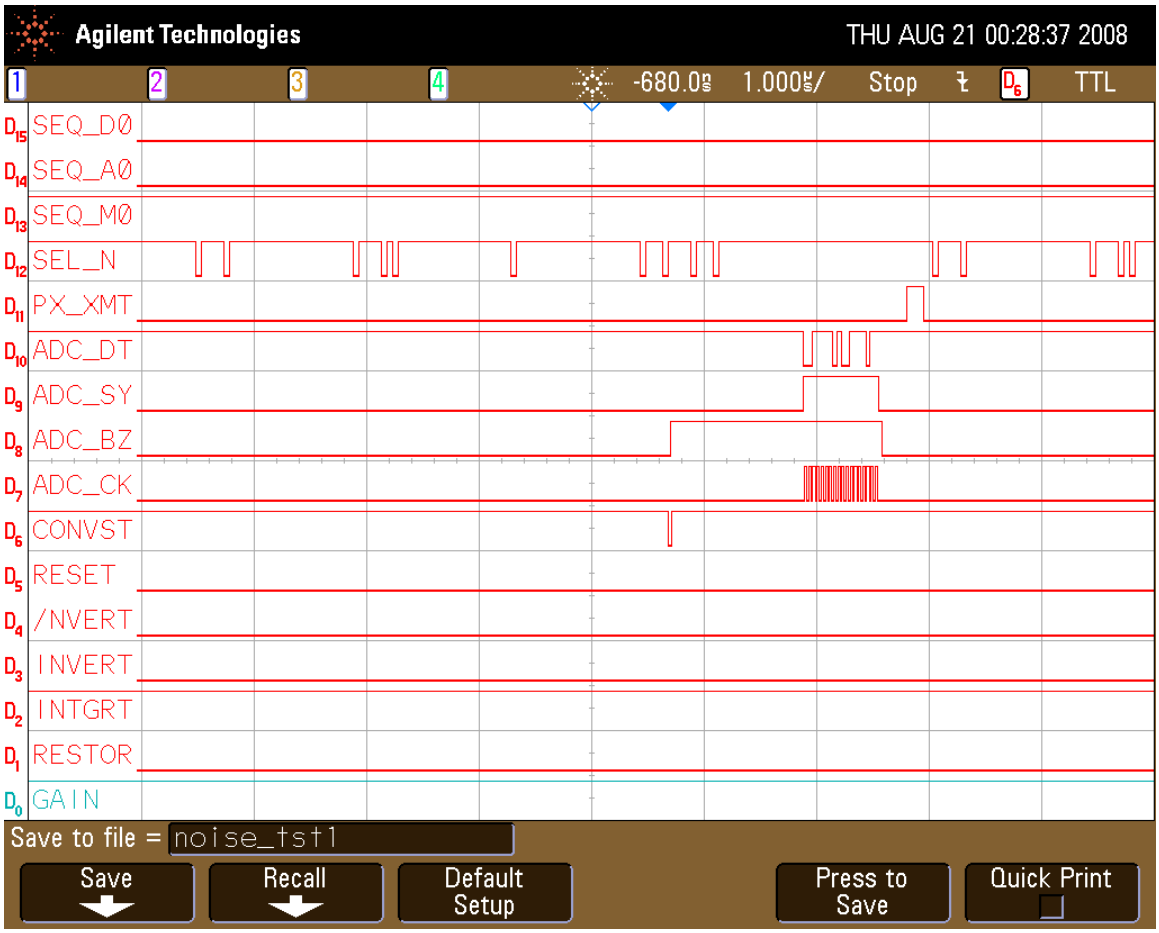

Figure 12 Waveform from Step ii, “Noise Test 1”

Step iii. Press the button marked >***Noise Test 2***< to do another conversion. This time the gain stage, phase inverter and integrator are run in a normal fashion while still holding the DC Clamp switch on. In this way the dynamic noise of the circuit can be measured up to the input of the gain stage (without the pre-amp). The scope will capture another waveform that should look similar to Figure 13. The results of the conversion and analysis are written to the log file.

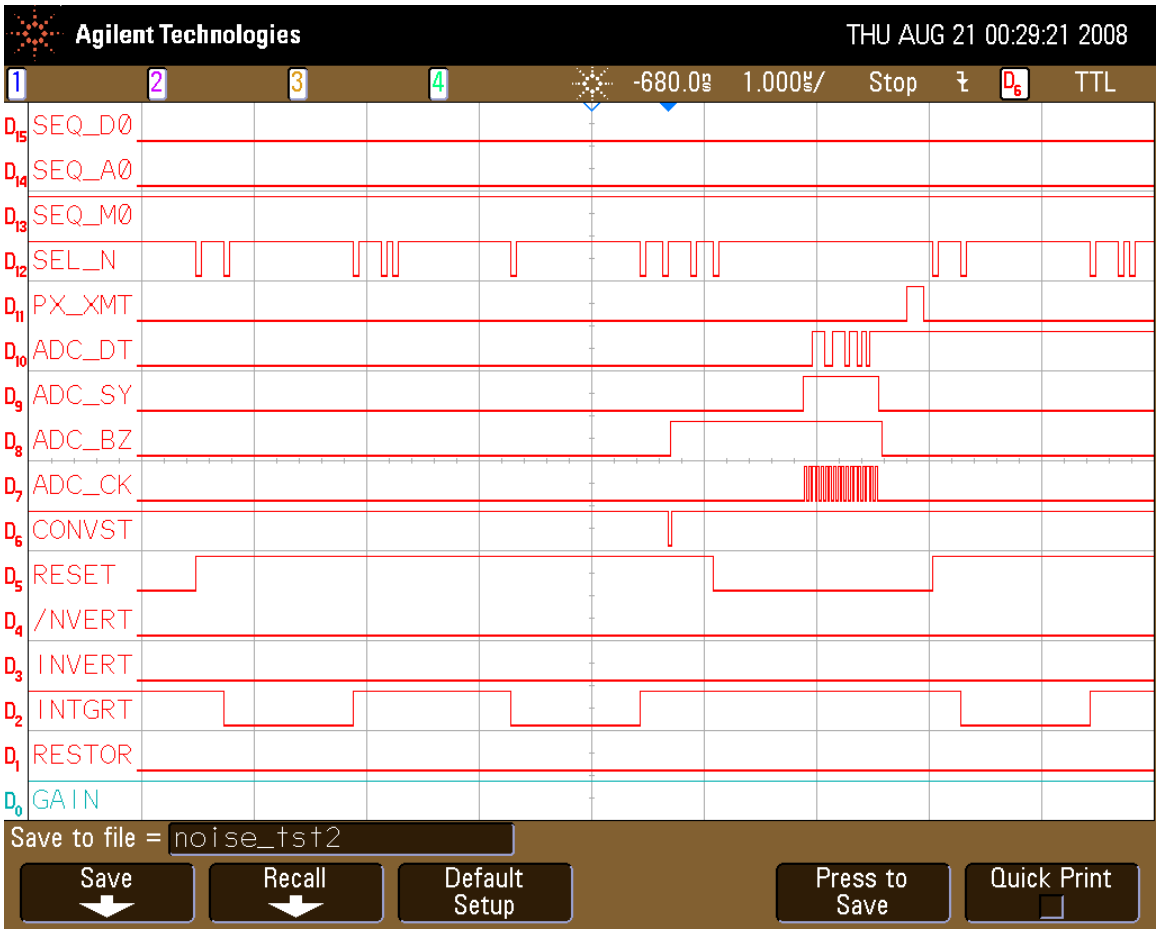

Figure 13 Waveform from Step iii, "Noise Test 2"

Step iv. Press the button marked >***Noise Test 3***< .This test shows that the inverted / non-inverted phase switching of the signal is taking place. The acquisition process should finish without error and the data is analyzed and written to the screen and to the log file. The waveform on the screen should resemble the screenshot shown in figure 14.

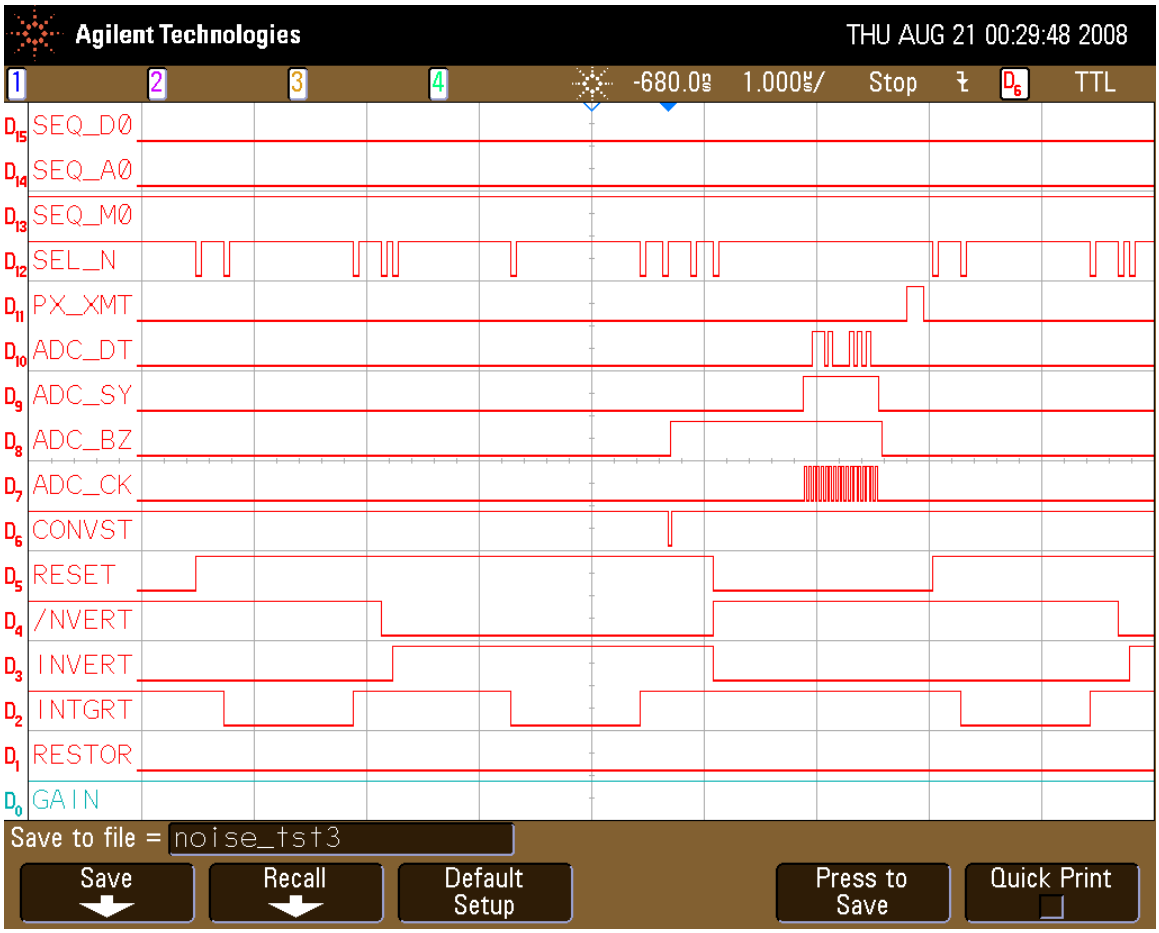

Figure 14 Waveform from Step iv, "Noise Test 3"

Step v. Press the button marked ***>Noise Test 4<*** to acquire another file. This time the DC Restore signal is released and a normal acquisition cycle is demonstrated. The waveform should look similar to Figure 15.

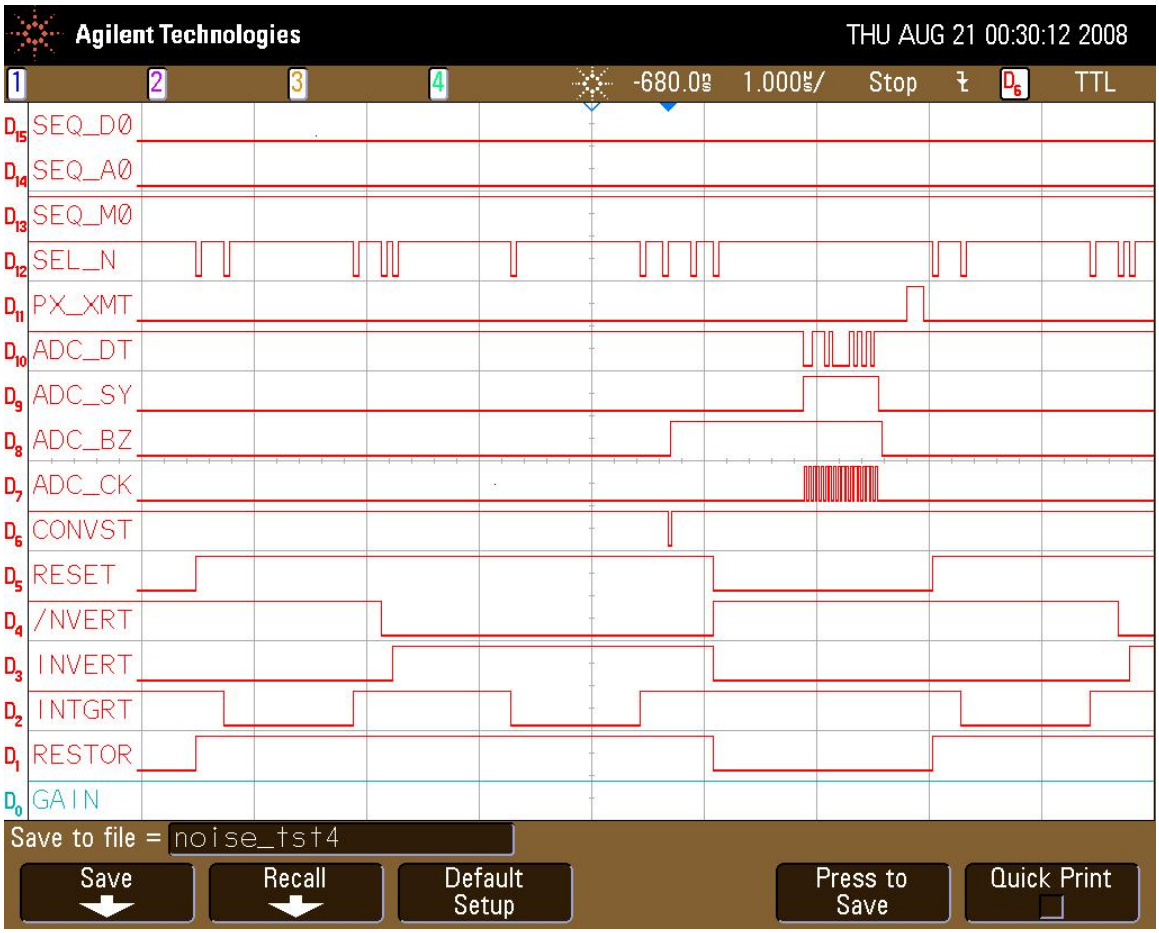

Figure 15 Waveform from Steps v, vi, vii, "Noise Test 4,5 and 6"

In the captured waveform in Figure 15, the DC Restore signal is shown toggling off for the complete pixel process time.

Step vi. Press the button marked ***>Noise Test 5<*** to acquire another file. This time the electronic gain is switched(low) into hi-gain mode. The captured waveform should look exactly like the previous acquisition with the exception of Gain signal being low (Figure 15).

Step vii. Press the button marked ***>Noise Test 6<***. The data generated from this test is used to verify the offset DAC stability. For this test the Offset DAC is adjusted from 10% to 90% in 10% increments, at each level the data is analyzed and reported into the log file. When the data is transferred from the log file to the EXCEL Spreadsheet a bar graph is generated for each of the 12 channels. The bar graph should show a linear increase in the value of the ADC conversions.

Step viii. Using the Signal Generator and oscilloscope connect up the test circuitry as shown in figure X(Scope Ext trigger output to Generator Trigger input on back of both units). Recall the setup file SETUP_0 to the Oscilloscope from the USB Thumb drive.

For the generator setup press the ARB button and then in the screen press the “Select Wform” button, followed by “Stored Wform” button. The ARB Mem1 should have the CCDSIM25 name, press the Select ARB button again. Next press the Store/Recall button, followed by the “Recall State” selection. State 1 should have CCD12A associated with it, press the “Recall State” button to select it. The Output button needs to be on to get the signal.

Connect the Signal generator output to the Test Board ADC ‘input 0’. Connect a cable between the 12 channel board front panel ‘output 0’and the oscilloscope analog input. Press the ***>Noise Test 4***< button. The analyzed results will be displayed in the window and also written to the log file, the analog input under test should have a value XXX counts above the other channels. The oscilloscope should display the waveforms similar to figure x. Repeat the test for all 12 channels, moving the cable between the oscilloscope and 12 channel board in step with the cable between the signal generator and the test board.

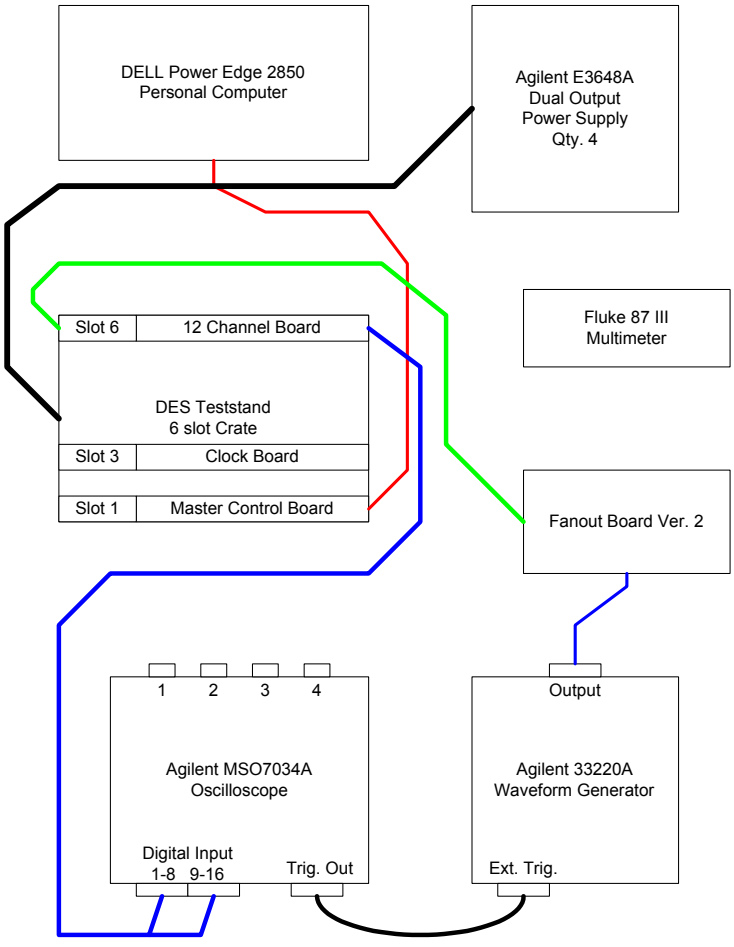

Figure 16 Test setup diagram

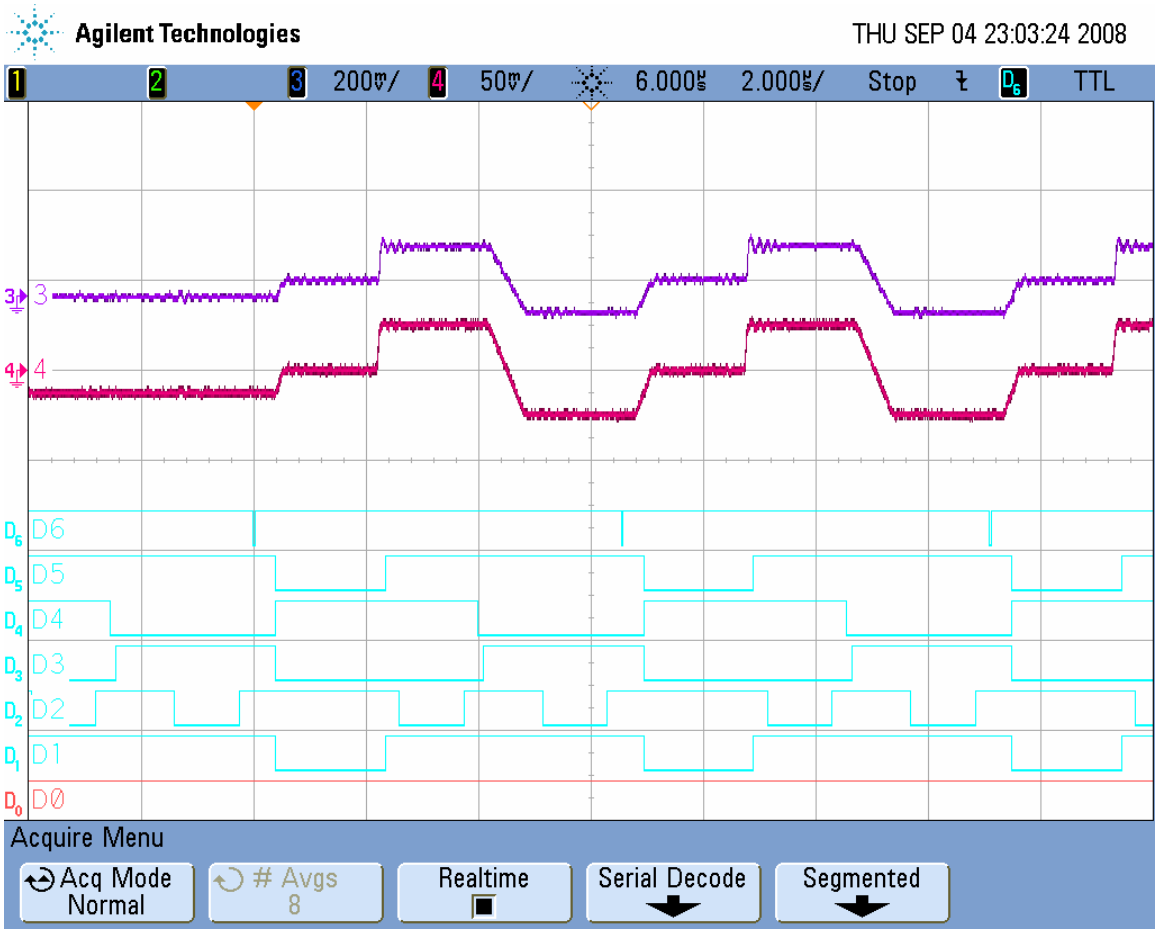

Figure 17 – Waveform results from Step Viii. Analog Input vs Analog Front Panel output.

Return to Stage 8 and complete Step x. on page 18.

Stage 12. Front-end Electronics Performance Analysis.

Step i. Input the data from the log file into the EXCEL spreadsheet using a cut and paste method.

Step ii. Results should be less than 7 ADU rms for each channel. Annotate the results of each channel's mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.

Plots should show consistent data spreads and no oscillation of levels. *Use the value of 1 for the column sub-region prompt and a value of 16 for the row sub-region prompt. Annotate the results of each sub-region for each channel's mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.*

Stage 13. Other Bit tests.

Step i. Select the “Other Bit Tests” button, a new window will appear. Click the “Read Register” button. The results of the following registers are written to the screen and also to the log file if the box was checked.
Firmware Version Registers – Currently we are at v2023
SERNUM register – This is a 32 bit number.
Ident Register – This should read back as 502hh
CCD Temp register – Value should be about room temperature ~ 25 degrees celcius

NOTE: The board can now be considered fully functional. Make sure that the filename for the **TEST SHEET** correctly reflects the product code and serial number of the board and store it in the **\\decapod\MonsoonAdmin\Production\TST_Repository\TestResults** directory**.** Make an Acrobat .pdf copy of the same file and store it in the **\\decapod\MonsoonAdmin\Production\HIST_Repository** directory.

2.0 Appendix

JTAG usage and Field Programmable Device (FPD) setup.

2.1 Appendix I CCD Acquisition Board FPD Programming

Step i. Connect the JTAG cable to the JTAG connector on the CCD Acquisition board. With power applied to the board, check that the status LED on the programming pod shows green. If not, the JTAG plug may be reversed. The +3.3V signal line for the JTAG socket is the one closest to the reset button. When the pod LED shows green, initialize the JTAG chain with the Xilinx IMPACT program.

Step ii. Follow the default prompts to launch the tool in its configuration mode. You may need to right click the mouse and select 'initialize chain' to connect to the CCD Acquisition board JTAG chain. After initialization two devices should be present on the JTAG chain. Figure XX shows a representative view. Further information on this tool can be found at: http://toolbox.xilinx.com/docsan/xilinx4/pdf/docs/pac/pac.pdf

Step iii. The Xilinx IMPACT application will ask you to select the appropriate files for each of the 2 devices. Use Table 3 to identify the correct load files. These files should be available from the local computer. If the IMPACT tool does not present a file menu to select the 'File' menu and click 'initialize chain' to accomplish this part.

Step iv. Place the mouse cursor over the first device icon (18V02) and right click. Select 'Program' and accept the default conditions (Erase before programming and Verify after programming). The tool will program the EEPROM device.

Step vi. If the board has not been programmed previously, power the complete board off and power on again to load the EEPROM boot contents to the Virtex device. If the board has been programmed previously, the front panel reset button can be used to re-boot the Virtex devce. Once the board has re-booted, right click on the second device icon (XC300E) and select **verify**. The verify cycle should complete without errors.

Step vii. The respective device checksums and user codes can be recovered from the devices by using the correct menu item after right clicking the respective device icon.

Step viii. Close the IMPACT tool application and disconnect the JTAG cable.

2.2 Appendix II. CCD Acquisition Board Power Supply Requirements

These tables outline the power consumption for the test chassis under test conditions:

2.2.1 Power Consumption Tables with only 12 Channel DES Acquistion board and Transition board in crate.

Table 7 - Power Supply Requirements (After Programming)

Supply Name	Set Voltage	Current reading	Over Current Setting
+3.3v Digital			
+5.0v Digital			
+5.0v Analog			
-5.0v Analog			
+15.0v Analog			
-15.0v Analog			
+28.0v Analog			

2.2.2 Power Consumption Tables with Master Control Board, Clock board and Clock Transition board along with the 12 Channel DES Acquistion board and Transition board

Table 8 - Power Supply Requirements (After Programming)

Supply Name	Set Voltage	Current reading	Over Current Setting
+3.3v Digital			
+5.0v Digital			
+5.0v Analog			
-5.0v Analog			
+15.0v Analog			
-15.0v Analog			
+28.0v Analog			

Still to do –
Make a doc that shows the waveform through the CDS section.
Do tests with appropriate Transition module.